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SINCE 2008

PRODUCTOUTLINE

SGC73050

Features

- LDO Low Noise Low-Dropout regulator
- Low IQ: 50 uA
- Available in multiple output versions: fixed and 4-8 bit programmable
- Maximum output current: 50 mA
- Ultra-high PSRR: 80 dB @ 20kHz; 70 dB @ 100kHz; 50 dB @ 1MHz
- Low Noise: 20 uV typical (20Hz to 20kHz)
- Large input range, from 1.8 V to 5.5 V
- Soft start and overcurrent protection
- Core area : 0.08 mm2

General Description

LDO: The SGC73050 is the 50 mA regulator of a family of low-dropout (LDO), low-power linear regulator IP solutions for integration on SoC offers very high power supply rejection ratio (PSRR). The family uses advanced control techniques to achieve soft start-up, very low noise, excellent transient response, and excellent PSRR performance. The SGC73050 is stable with a 1.0 uF ceramic output capacitor. It is specified from TJ = 40°C to +125 °C and is designed to achieve 3% overall accuracy (over Load/Line/Temp).

Applications

Quick Reference

LABEL	
V_{VREF}	V_{AB}

Applications Diagram