SILICONGATE
Powering your Success

COMMITMENT TO CUSTOMER SUCCESS SINCE 2008

PRODUCTOUTLINE

SGCADCSW_01_TSMC_CLN40ULP

ADC VOLTAGE CONDITIONER / DIVIDER

Features

- Input voltage conditioning
- Output voltage limiting
- 5V Tolerant input sense
- NMOS design
- Guaranteed 0V outputs when no supply is available
- Differential signaling disable

General Description

SGCADCSW_01_TSMC_CLN40ULP is an ADC signal conditioner / divider that guarantees 0V outputs when no supply is available or when the status of the supplies is unknown. It offers two voltage dividers (1/1.8 and 1/5.5) that can be controlled with an enable pin. The *SGCADCSW_01_TSMC_CLN40ULP* is specified from TJ = -40°C to 125°C and can be found as isolated IP or integrated into *PMUs*, as for example in the *SGCPMU_01_TSMC_CLN40ULP*.

Applications

- ADC signal conditioner/divider

Quick Reference

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{VDDH}	Gate Driver Supply	2.1	2.4	3.6	V
V_{DVDD}	Digital Supply	0.55	-	1.21	V

Applications Diagram

2021-03-22 00:00:00
2020-11-16 00:00:00